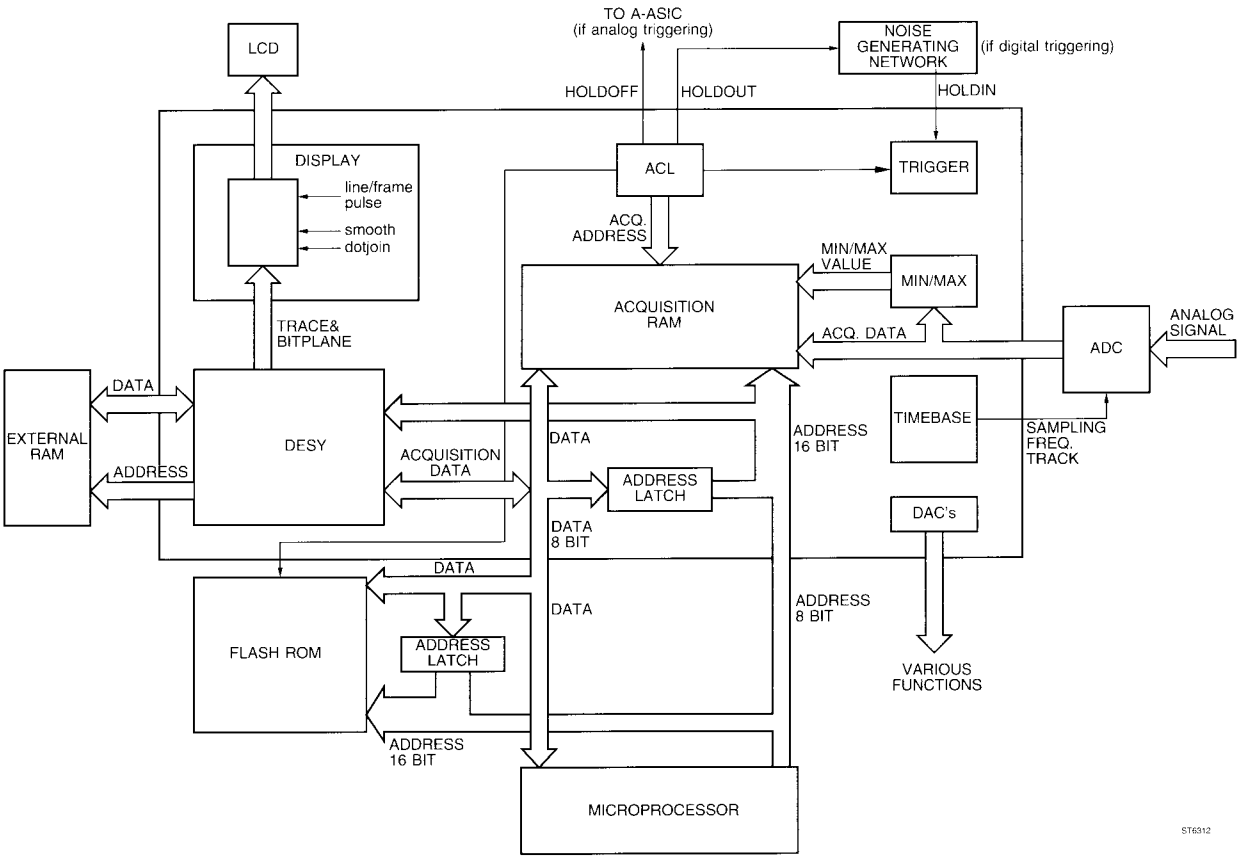

Figure 3.4 Schematic Diagram D-ASIC D1203

Acquisition Control Logic (ACL)

The ACL controls the analog input circuitry and the ADC (N2302, see circuit diagram A2a/A2b, figure 10.5/10.6). The ACL also writes the digital representations of the input signals to the Acquisition RAM in the D-ASIC, according to the selected trigger and acquisition modes. Before the acquired trace data is displayed, it is first processed by the microprocessor. The microprocessor corrects for offset- and amplification errors, using the calibration values that are stored in Flash ROM.

In fast timebase positions the ACL acquires 1024 values. Then the acquisition is stopped and the microprocessor can read the data out of the Acquisition RAM. In slow timebase positions the ACL uses the Acquisition RAM as a FIFO (First In First Out) memory. The microprocessor can start reading the acquired data immediately after triggering. Now there is synchronization between the ACL and the microprocessor.

If the system uses analog triggering (time base $\geq 1\mu s$), the trigger hold-off signal (HLDOFFN) to the A-ASIC is generated. In digital triggering mode, the D-ASIC generates the HLDOUTN signal. This signal is fed to the HLDIN input of the D-ASIC, via R1211, C1221, R1214 and C1211. These components generate noise on the HOLDOUTN signal, which is needed as a random factor in the Delta- T circuit.

Min/max

The Min/max module finds the minimum and maximum value of the input signals between two time base pulses, and writes them into the Acquisition RAM. To detect narrow glitches, the TRACK signal (ADC sample frequency) is always 25 MHz in Min/max mode.